IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Assignee:	Intel Corporation
Inventor:	VANDENTOP, Gilroy J. et al.
Application No.:	10/020,911
Filed:	December 19, 2001
TC/Art Unit:	2827
Examiner:	ZARNEKE, DAVID A.
Docket No.:	2207/12665
Customer No.	23838
Serial No.:	10/020,911
Title:	ELECTRICAL/OPTICAL INTEGRATION SCHEME USING DIRECT COPPER BONDING

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

RESPONSE AND REQUEST FOR RECONSIDERATION

In response to the Office Action mailed on October 10, 2003, Applicants submit the following remarks.

REMARKS

Claims 1-4, 14-16 and 31 are pending in the application. Claims 5-13 and 17-30 have been withdrawn from consideration.

Claims 1-4, 14-16 and 31 have been rejected under 35 U.S.C. §103(a) over what has been described as "Applicant's admitted prior art" and Fan et al., "Copper Wafer Bonding",